STIC Search Report
EIC 2800

STIC Database Tracking Number: 130404

TO: Monica Lewis **Location: JEF 5A30** **Art Unit : 2822** **Tuesday, August 24, 2004** **Case Serial Number: 09/805027**	**From: Scott Hertzog** **Location: EIC 2800** **JEF4B68** **Phone: 272-2663** **Scott.hertzog@uspto.gov**

Search Notes

Examiner Lewis,

Attached are edited first pass search results from the patent and nonpatent databases.

Colored tags indicate abstracts especially worth your review.

If you need further searching or have questions or comments, please let me know.

Thanks,
Scott Hertzog

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     INDEX 'HCAPLUS, INSPEC, COMPENDEX, WPIX, JICST-EPLUS' ENTERED AT 15:55:22
     ON 24 AUG 2004
L1             QUE 7429-90-5 OR AL OR ALUMINUM OR ALUMINIUM
L2             QUE 7440-50-8 OR COPPER OR CU
L3             QUE 7440-33-7 OR TUNGSTEN OR W
L4             QUE 12033-62-4 OR TANTALUM(A) NITRIDE OR TAN
             531   FILE HCAPLUS
               7   FILE INSPEC
               6   FILE COMPENDEX
             397   FILE WPIX
               3   FILE JICST-EPLUS
L5             QUE L1 AND L2 AND L3 AND L4
L6             QUE VIA OR STUD OR INTERCONNECT? OR INTER(W)CONNECT?
L7             QUE LINING OR LINER OR LINED
L8             QUE PVD OR VAPOR DEPOSITION PROCESS(L) PHYS/CT OR ((PHYS OR
                 PHYSICAL)(A)(VAPOR OR VAPOUR))(A) DEPOSIT? OR SPUTTER?
              10   FILE HCAPLUS
              15   FILE WPIX
L9             QUE L5 AND L6 AND L7 AND L8
L10            QUE L3(3N) L6
              44   FILE HCAPLUS
               8   FILE INSPEC
               6   FILE COMPENDEX
              40   FILE WPIX
               1   FILE JICST-EPLUS
L11            QUE L4(3N) L7
               7   FILE HCAPLUS
               6   FILE WPIX
L12            QUE L9 AND (L10 OR L11)
L13            QUE L8(L) L3
               ---------
               SEA L8(S)L3
               ---------
               0*  FILE HCAPLUS
L14            QUE L9 AND L13
L15            QUE L12 OR L14
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     FILE 'WPIX, HCAPLUS' ENTERED AT 16:09:50 ON 24 AUG 2004
L16          22 S L15
L17          19 DUP REM L16 (3 DUPLICATES REMOVED)
                   ANSWERS '1-15' FROM FILE WPIX
                   ANSWERS '16-19' FROM FILE HCAPLUS
L18           0 S L17 NOT P/DT NOT PY>2001
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130404

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 8/20/04 Serial # 09/805,027 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2822 Phone 272-1935 Room 5A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

Need before 8/25

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or **Information Disclosure Statements.** _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ____

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-3, 5-7, 9 & 10

Please also look for the materials that are disclosed

Problem: See pages 2-5

Solution: " " 6

Staff Use Only		Type of Search		Vendors	
Searcher:	Scott Hertzog	Structure (#)		STN	
Searcher Phone:	2-2663	Bibliographic	✓	Dialog	
Searcher Location:	STIC-EIC2800, JEF-4B68	Litigation		Questel-Orbit	
Date Searcher Picked Up:	8/24/4	Fulltext		LexisNexis	
Date Completed:	8/24/4	Patent Family		WWW/Internet	
Searcher Prep/Rev Time:	136	Other		Other	
Online Time:	86				

☐ **L17 ANSWER 1 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN DUPLICATE 1**

Accession Number

2004-468072 [44] WPIX Full Text

Title

Depositing metal layer on interconnect structure, e.g. vias , for semiconductor wafer, comprises patterning dielectric layer to form opening, depositing liner layer, sputter -etching liner layer, and depositing additional layer(s).

Author/Inventor

MALHOTRA, S G; SIMON, A H; MALHOTRA, S; SIMON, A

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM DEUT GMBH

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2004115928	A1	20040617	(200444)*		7	H01L021-4763
WO 2004053926	A2	20040624	(200444)	EN		H01L000-00

Priority Application Information

US 2002-318605	***20021211***

International Patent Classification

ICM H01L000-00; H01L021-4763

Abstract

US2004115928 A UPAB: 20040712

NOVELTY - A metal layer is deposited on an ***interconnect*** structure for a semiconductor wafer by providing an ***interconnect*** structure comprising a metallic conductor (14) covered by a dielectric layer (12, 18), patterning the dielectric layer to form an opening, depositing a ***liner*** layer (24) on the opening, ***sputter*** -etching the ***liner*** layer, and depositing an additional layer(s) (26) on the wall of the opening.

DETAILED DESCRIPTION - Depositing a metal layer on an ***interconnect*** structure for a semiconductor wafer comprises providing an ***interconnect*** structure comprising a metallic conductor covered by a dielectric layer, patterning the dielectric layer to form an opening that exposes the metal conductor, depositing a ***liner*** layer on a wall and bottom of the opening, ***sputter*** -etching the ***liner*** layer to expose the metal conductor and partially redepositing the ***liner*** layer on a sidewall of the opening, and depositing an additional layer(s) on the wall of the opening and covering the redeposited ***liner*** layer.

USE - Used for depositing metal layer on an ***interconnect*** structure, e.g. ***vias*** , trench, and pads, for a semiconductor wafer.

ADVANTAGE - The process provides improved electromigration resistance and reduced stress migration and avoids time dependent dielectric breakdown.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional side view of the semiconductor wafer.

Dielectric layer 12, 18

Metallic conductor 14

Liner layer 24

Additional layer 26

Dwg.1D/2

Technology

US 2004115928 A1UPTX: 20040712 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: The opening is filled with ***copper***. Depositing the ***liner*** layer, the additional layer(s), and the wafer are exposed to an airbreak.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The ***liner*** layer

comprises ***tantalum nitride*** (***TaN***), tantalum (Ta), titanium (Ti), titanium(silicon) nitride (Ti(Si)N), or ***tungsten*** (***W***). The additional layer(s) comprises ***TaN*** , Ta, Ti, Ti(Si)N, ***W*** , or ***copper*** . The metal conductor comprises ***copper*** , ***tungsten*** , or ***aluminum***. Preferred Component: The gas for ***sputter*** etching is argon, helium, neon, xenon, nitrogen gas, hydrogen gas, ammonia, and/or nitrogen hydride.

☐ **L17 ANSWER 2 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN DUPLICATE 2**

Accession Number

2004-468071 [44] WPIX Full Text

Title

Depositing metal layer on interconnect structure, e.g. pads, for semiconductor wafer, comprises patterning dielectric layer to form opening, sputter -etching capping layer, and depositing layer(s) on wall of opening.

Author/Inventor

CLEVENGER, L; DALTON, T J; HOINKIS, M; KALDOR, S K; KUMAR, K; LA TULIPE, D C; SEO, S; SIMON, A H; WANG, Y; YANG, C; YANG, H; DALTON, T; KALDOR, S; LA TULIPE, D; SIMON, A

Patent Assignee/Corporate Source

(INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM DEUT GMBH; (INFN) INFINEON TECHNOLOGIES AG

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2004115921	A1	20040617	(200444)*		8	H01L021-4763
WO 2004053979	A1	20040624	(200444)	EN		H01L021-768

Priority Application Information

US 2002-318606	***20021211***

International Patent Classification

ICM H01L021-4763; H01L021-768
ICS H01L021-44

Abstract

US2004115921 A UPAB: 20040712

NOVELTY - A metal layer is deposited on an ***interconnect*** structure for a semiconductor wafer by providing an ***interconnect*** structure comprising a metallic conductor (14) covered by capping layer and a dielectric layer (12, 18), patterning the dielectric layer to form an opening, ***sputter*** -etching the capping layer, and depositing a layer(s) (26) on the wall of the opening.

DETAILED DESCRIPTION - Depositing a metal layer on an ***interconnect*** structure for a semiconductor wafer comprises providing an ***interconnect*** structure comprising a metallic conductor covered by a capping layer and a dielectric layer, patterning the dielectric layer to form an opening that exposes the capping layer over the metal conductor, ***sputter*** -etching the capping layer to expose the metal conductor and partially redepositing the capping layer on a sidewall of the opening, and depositing a layer(s) on the wall of the opening and covering the redeposited capping layer.

USE - Used for depositing a metal layer on an ***interconnect*** structure, e.g. pads, for a semiconductor wafer.

ADVANTAGE - The process provides improved electromigration resistance and reduced stress migration and avoids time dependent dielectric breakdown.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional side view of the semiconductor wafer.

Dielectric layer 12, 18
Metallic conductor 14

Liner layer 24 Layer(s) 26
Dwg.1E/2

Technology

US 2004115921 A1UPTX: 20040712 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: A ***liner*** layer (24) is deposited on a wall and bottom of the opening. The ***liner*** layer is also ***sputter*** -etched to expose the capping layer and partially redeposited on a sidewall of the opening. The opening is filled with ***copper***. Preferred Component: The opening is a ***via*** or a trench.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The capping layer is silicon nitride, silicon carbide, silicon oxycarbide, hydrogenated silicon carbide, or silicon dioxide. The layer(s) and the ***liner*** layer comprise ***tantalum nitride*** (***TaN***), tantalum (Ta), titanium (Ti), titanium(silicon) nitride (Ti(Si)N), or ***tungsten*** (***W***). The metal layer(s) comprises ***TaN*** , Ta, Ti, Ti(Si)N, ***W*** , or ***copper*** . The metal conductor comprises ***copper*** , ***tungsten*** , or ***aluminum***. Preferred Component: The gas for ***sputter*** etching is argon, helium, neon, xenon, nitrogen gas, hydrogen gas, ammonia, and/or nitrogen hydride.

TECHNOLOGY FOCUS - CERAMICS AND GLASS - Preferred Material: The capping layer may comprise an organosilicate glass.

☐ **L17 ANSWER 3 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN DUPLICATE 3**

Accession Number

2002-740392 [80] WPIX Full Text

FYI - Instant Application

Title

Integrated circuit has patterned copper layer, patterned aluminum layer, stud connection in opening between locations on patterned layers, and liner extending between stud connection and location on patterned copper layer.

Author/Inventor

BURRELL, L G; COONEY, E E; GAMBINO, J P; HEIDENREICH, J E; LEE, H K; LEVY, M D; LI, B; LUCE, S E; MCDEVITT, T L; STAMPER, A K; WONG, K H; YANKEE, S J

Patent Assignee/Corporate Source

(BURR-I) BURRELL L G; (COON-I) COONEY E E; (GAMB-I) GAMBINO J P; (HEID-I) HEIDENREICH J E; (LEEH-I) LEE H K; (LEVY-I) LEVY M D; (LIBB-I) LI B; (LUCE-I) LUCE S E; (MCDE-I) MCDEVITT T L; (STAM-I) STAMPER A K; (WONG-I) WONG K H; (YANK-I) YANKEE S J

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002127846	A1	20020912	(200280)*		6	H01L021-4763

Priority Application Information

US 2001-***805027***	***20010312***

International Patent Classification

ICM H01L021-4763

Abstract

US2002127846 A UPAB: 20021212
NOVELTY - Integrated circuit comprises a patterned ***copper*** layer, a patterned ***aluminum*** layer, a ***stud*** (50) connection in an opening between a location on the patterned ***copper*** layer and a location on the patterned ***aluminum*** layer, and a ***liner*** (40) in the opening and extending between the ***stud*** connection and the location on the patterned ***copper*** layer.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the production of an interface structure between ***copper*** and ***aluminum*** metallurgy layers in an integrated circuit, which comprises covering a ***copper*** metallurgy layer with an

insulator, forming an opening through the insulator to the ***copper*** metallurgy layer, forming a ***liner*** of a conductive barrier material in the opening, filling a remainder of the opening with a conductive material to form a ***stud*** , and forming a patterned ***aluminum*** metallurgy layer over the ***stud***.

USE - Used as an integrated circuit.

ADVANTAGE - The integrated circuit provides a ***copper*** to ***aluminum*** interface structure which allows ***interconnections*** and/or solder or wire bond pads to be formed in the same layer, allowing substitution of a layer of ***aluminum interconnects*** for a layer of ***copper interconnects*** , improving performance, reducing fabrication time, increasing tool throughput, and thus reducing integrated circuit costs, while avoiding deleterious effects of process materials on ***copper*** which can compromise performance and/or reliability of the integrated circuit.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of an integrated circuit.

Liner 40

Stud 50

Solder or wire bond connection pads 105 Dwg.1/2

Technology

US 2002127846 A1UPTX: 20021212 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: The step of forming the ***liner*** includes chemical vapor deposition of ***tantalum nitride*** and ***tungsten*** , respectively. The method further includes forming a covering layer over the patterned ***aluminum*** layer. The patterned ***aluminum*** layer includes ***interconnects*** and solder or wire bond connection pads (105), and the method further includes opening the covering layer at the solder or wire bond connection pad. The method also includes forming a barrier layer over the ***copper*** metallurgy layer.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Components: The ***liner*** comprises a layer of ***tantalum nitride*** and a layer of ***physical vapor deposition*** (***PVD***) ***tungsten***. It may comprise a layer of titanium and a layer of titanium nitride or ***PVD tungsten***. The ***stud*** connection is formed of ***tungsten***. The patterned ***aluminum*** layer includes a layer of at least one of titanium and titanium nitride. The integrated circuit includes a covering layer including a layer of silane-based high density plasma oxide.

☐ **L17 ANSWER 4 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2004-009885 [01] WPIX Full Text

Title

Interconnect structure for high speed microprocessors includes substrate having patterned dielectrics including porous low dielectric constant separated by buried etch stop layer, polish stop and metal conductor.

Author/Inventor

GATES, S M; HEDRICK, J C; NITTA, S V; PURUSHOTHAMAN, S; TYBERG, C S

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003183937	A1	20031002	(200401)*		12	H01L047-02

Priority Application Information

US 2001-795431	**20010228**
US 2003-396274	20030325

International Patent Classification

ICM H01L047-02

Abstract

US2003183937 A UPAB: 20040102

NOVELTY - An ***interconnect*** structure comprises a substrate (50) having a patterned multilayer of dielectrics including:

(a) porous low dielectric constant (k) dielectrics (54, 58) which are separated from each other by a buried etch stop layer (56);

(b) a polish stop formed on the patterned multilayer of spun-on dielectrics (52') on the second porous low k dielectric; and

(c) a metal conductor (74) formed within the patterned multilayer of dielectrics.

DETAILED DESCRIPTION - An ***interconnect*** structure comprises:

(a) a substrate having a patterned multilayer of dielectrics including first and second porous low k dielectrics which are separated from each other by a buried etch stop layer, the porous low k dielectrics having a first composition and the buried etch layer having a second composition which is different from the first composition;

(b) a polish stop formed on the patterned multilayer of spun-on dielectrics on the second porous low k dielectric; and

(c) a metal conductor formed within the patterned multilayer of dielectrics.

An INDEPENDENT CLAIM is also included for a method of fabricating low k dielectric plus metal conductor ***interconnect*** structure comprising:

(a) forming a multilayer of spun-on dielectric on a surface;

(b) forming a hard mask on the spun-on dielectrics, the hard mask including a polish stop layer and a patterning layer on the polish stop layer;

(c) forming an opening in the hard mask to expose a surface of the spun-on dielectrics;

(d) forming a trench in the exposed surface using the hard mask as an etch mask;

(e) filling the trench with a conductive metal; and

(f) planarizing the conductive metal stopping on the polish stop layer.

USE - Used for high speed microprocessors, application specific integrated circuits and other high speed integrated circuits.

ADVANTAGE - Provides precise and uniform control over the metal conductor resistance so improving reliability without added processing cost.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the ***interconnect*** structure. Substrate 50

Spun-on dielectrics 52'

Porous low k dielectrics 54, 58

Buried etch stop layer 56

Metal conductor 74

Dwg.8/8

Technology

US 2003183937 A1UPTX: 20040102 TECHNOLOGY FOCUS - ORGANIC CHEMISTRY - Preferred Component: The first and second porous low k dielectrics are organic dielectrics having a pore size of 1-50 nm at 5-35 vol.% porosity. The first and second porous low k dielectrics comprise carbon, oxygen and hydrogen. The buried etch stop layer is an inorganic low k dielectric material or an inorganic/organic hybrid material. The buried etch stop layer comprises silsesquioxane HOSP, methyl silsesquioxane (MSQ), tetraethylorthosilicate, hydrosilsesquioxane (HSQ), MSQ-HSQ copolymers, organosilanes or any other silicon-containing material. Preferred Property: The first and second low k dielectric have a dielectric constant of 1.1-3.5, preferably 1.4-3. Preferred Property: The inorganic low k dielectric material has a pore size of 5-500 Angstrom at 5-80 vol.% porosity. TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The substrate is a

semiconductor wafer having an adhesion promoter layer. Preferred Method: The spun dielectrics are cured at 250-500 degreesC for 30-500 seconds. The hard mask is formed by plasma enhanced chemical vapor deposition or by spin-on coating. The trench is formed by reactive ion etching, ion beam etching or plasma etching. The trench fill includes chemical vapor deposition (CVD), plasma-assisted CVD, plating, ***sputtering*** or chemical solution deposition. The conductive metal is planarized by chemical-mechanical polishing.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The metal conductor is composed of ***aluminum*** , ***copper*** , ***tungsten*** and/or silver. The ***liner*** material comprises titanium ***nitride*** , ***tantalum nitride*** , titanium, tantalum, ***tungsten*** , ***tungsten*** nitride, chromium and/or niobium.

☐ **L17 ANSWER 5 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-371143 [35] WPIX Full Text

Title

Fabrication of integrated circuit on substrate, by depositing alloyed thin seed layer by physical vapor deposition followed by chemical vapor deposition, or electrochemical deposition of thick layer of pure copper , and annealing.

Author/Inventor

CHEN, S; TSAI, M

Patent Assignee/Corporate Source

(TASE-N) TAIWAN SEMICONDUCTOR MFG CO

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003022480	A1	20030130	(200335)*		7	H01L021-4763

Priority Application Information

US 1999-412632	**19991004**
US 2002-253691	20020924

International Patent Classification

ICM H01L021-4763

ICS H01L021-302; H01L021-461

Abstract

US2003022480 A UPAB: 20030603

NOVELTY - An integrated circuit on a substrate (20) is fabricated by:

(i) depositing an alloyed thin seed layer by ***physical vapor deposition*** (***PVD***), followed by chemical vapor deposition (CVD) or electrochemical deposition (EC) of a thick layer of pure ***copper*** ; and

(ii) annealing by separate low temperature to enhance ***copper*** alloy formation.

DETAILED DESCRIPTION - Fabrication of an integrated circuit on a substrate, comprises:

(a) providing a substrate or substrate module;

(b) a substrate having a layer of dielectric, interlevel dielectric (ILD), or an ***interconnect*** line layer, or device contact region to P-N junctions;

(c) a first level of conducting wiring defined and embedded in a first layer of insulator (22);

(d) patterned and etched ***via*** holes and trenches (channels) (23) in a deposited insulating material (24);

(e) depositing (blanket) a thin ***via*** hole and trench barrier ***liner*** material, which is a diffusion barrier;

(f) (alternate M1) depositing an alloyed thin seed layer by ***PVD*** followed

by CVD, or ECD of a thick layer of pure ***copper*** (26); or

(g) (alternate M2) depositing a thick layer of pure ***copper*** by CVD or ECD followed by an alloyed layer by ***PVD*** ;

(h) annealing by separate low temperature for M1 and M2, to enhance ***copper*** alloy formation; and

(i) polishing the excess conducting metal back by chemical mechanical polishing (CMP) and repeating the process steps to make multilevel conducting layers.

USE - For fabrication of integrated circuit on substrate.

ADVANTAGE - The method provides a unique ***copper*** metal alloyed conducting ***interconnect*** lines and ***via*** structures, having good fill properties for high aspect ratio ***vias*** and trenches, good adhesion properties with insulating films, and oxidation/corrosion and electromigration resistance, hence improving reliability. It results in less processing time, lower costs and higher device reliability.

DESCRIPTION OF DRAWING(S) - The figure illustrates in cross-sectional representation, the ***PVD*** ***sputtering*** of a ***copper*** alloy layer.

Substrate 20

Metal ***copper*** wiring 21

First layer of insulator 22

Trenches 23

Deposited insulating material 24

Thick layer of pure ***copper*** 26

Thin conformal alloy seed layer 27 Dwg.2b/2

Technology

US 2003022480 A1UPTX: 20030603 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Material: The substrate is semiconductor single crystal silicon or a ceramic module, with integrated circuits. Preferred Component: The trench or channel and ***via*** hole contact comprises a diffusion barrier ***liner*** , which aids adhesion. Preferred Condition: The annealing by separate low temperature annealing steps, depending on the metal stack structure, to enhance ***copper*** metal alloy formation is performed at 250-450degreesC. Preferred Method: Each level of conducting structure is planarized by removing excess conducting material, through CMP or etching.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Component: The ***liner*** type materials comprise ***tantalum*** ***nitride*** , titanium nitride, and ***tungsten*** nitride and can be formed by reactive ***sputtering***.

TECHNOLOGY FOCUS - METALLURGY - Preferred Component: The thin conformal alloyed seed layer (27) are composed of ***copper*** alloying metals, i.e., zirconium, ***aluminum*** , titanium, tin, zinc, or magnesium, ***sputtered*** from a target, which contains the alloyed material (***PVD***). Preferred Property: The thin conformal alloyed seed layer is 500-2500 Angstrom thick. The planarized trench/***via*** surface is 3000-15000 Angstrom thick.

☐ **L17 ANSWER 6 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-491814 [46] WPIX Full Text

Title

Formation of electrical connections on semiconductor wafer comprises depositing first conductive material in non-ionized deposition process into semiconductor wafer to line each aperture opening to underlying areas.

Author/Inventor

COONEY, E C; MURPHY, W J

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6534394	B1	20030318	(200346)*		19	H01L021-4763

Priority Application Information

US 2000-660711	**20000913**

International Patent Classification

ICM H01L021-4763

Abstract

US 6534394 B UPAB: 20030719

NOVELTY - Electrical connections are formed on a semiconductor wafer by depositing a first conductive material in a non-ionized deposition process into a semiconductor wafer to line each aperture opening to underlying areas, and depositing a second conductive material in an ionized deposition process into the semiconductor wafer.

DETAILED DESCRIPTION - Formation of electrical connection involves:

(a) providing a semiconductor comprising an insulating layer having apertures and covering a substrate;

(b) depositing a first conductive material in a non-ionized deposition process into the semiconductor wafer, ***lining*** each aperture; and

(c) after depositing the first conductive material, depositing a second conductive material in an ionized deposition process into the semiconductor wafer, additionally ***lining*** each aperture and forming a barrier comprising first and second conductive material ***linings*** with the first and second conductive materials comprising the same material.

USE - Used for forming electrical connections on a semiconductor wafer.

ADVANTAGE - The process creates robust contacts and ***interconnects*** by depositing a thin layer of conductive material on a wafer through a non-ionized deposition process. It avoids charge differentials caused by non-uniform plasmas, yet avoids a center thick deposition profile along the surface of the wafer. Metal interfaces created in aperture bases are not contaminated with oxide, fluorinated silica glass, SiLK or other dielectric or interposed material, thus eliminating high contact or ***via*** junction resistance. The invention can also augment and provide improvements to the sequentially deposited ***tantalum nitride /tantalum*** bilayer process.

DESCRIPTION OF DRAWING(S) - The figure is a flow diagram showing a method for creating robust contacts and ***interconnects***. Dwg.1/10

Technology

US 6534394 B1 UPTX: 20030719 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: A fill material is deposited into the semiconductor wafer until the fill material fills each aperture. A subtractive etching is performed to pattern the barrier (i.e., conductive film) and fill material. The conductive film and the fill material are polished down to the insulating layer. The non-ionized deposition process is a ***physical vapor deposition*** (***PVD***) process or a chemical vapor deposition process. The ***physical vapor deposition*** process further comprises providing an atmosphere containing nitrogen and providing a target comprising tantalum, titanium or ***tungsten***. The ionized deposition process is an ionized ***PVD*** process. The first and second conductive materials are deposited at an absolute pressure of 1-60 mTorr, -150-500degreesC, a gas flow of 1-150 sccm, and a power level of 100-10000 watts.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The first conductive material comprises nitrides of the target material. The conductive materials comprise tantalum, titanium, ***tungsten*** , ***copper*** , ***aluminum*** , cobalt,

copper alloy, ***aluminum*** alloy, or cobalt alloy.

☐ **L17 ANSWER 7 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-361862 [34] WPIX Full Text

Title

Integration of integrated circuit components in copper interconnects by forming spiral inductor, metal-insulator-metal capacitor and precision resistor within inductor area, capacitor area and resistor area, respectively.

Author/Inventor

HATZILAMBROU, M; JOHNSON, E; LEUNG, C; QIAN, Y; THEDOAN, M Y; YU, B; DOAN, M T

Patent Assignee/Corporate Source

(MICR-N) INST MICROELECTRONICS

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002197844	A1	20021226	(200334)*		24	H01L021-4763
US 6534374	B2	20030318	(200334)			H01L021-20
SG 98045	A1	20030820	(200362)			H01L021-4763

Priority Application Information

US 2001-876627	**20010607**

International Patent Classification

ICM H01L021-20; H01L021-4763

Abstract

US2002197844 A UPAB: 20030529

NOVELTY - Integrated circuit components in ***copper interconnects*** are integrated by dividing a wafer into a spiral inductor area, a metal-insulator-metal (MIM) capacitor area and a precision resistor area; and forming a spiral inductor within the spiral inductor area, a MIM capacitor within a MIM capacitor area and a precision resistor within a precision resistor area.

DETAILED DESCRIPTION - Integration of an integrated circuit component in ***copper interconnects*** includes providing a wafer having an exposed top-most planar ***copper interconnect***. The wafer is divided into one or more areas from: a spiral inductor area (12) having an exposed planar ***copper interconnect*** bottom half (22) of a stacked spiral inductor; a MIM capacitor area (14) having an exposed planar ***copper interconnect*** bottom plate (26) and exposed planar ***copper interconnect*** contact point (28) of a MIM capacitor; and a precision resistor area (16) having a two exposed planar ***copper interconnect*** routing points (24) of a precision resistor. A first insulator layer is formed over the structure. A metal layer is formed over the first insulator layer. A first patterned masking layer is formed over the metal layer covering a portion of the MIM capacitor area exposed planar ***copper interconnect*** bottom plate and a portion of the area between the precision resistor area planar ***copper interconnect*** routing points. The metal layer is etched over the first dielectric insulator layer, without etching the underlying first dielectric insulator layer, using the patterned first masking layer as a mask, to form a metal top plate over a portion of the ***interconnect*** bottom plate of the MIM capacitor and a patterned metal layer portion between the two planar ***copper interconnect*** routing points of the precision resistor. A second insulator layer is formed over the structure. A second patterned masking layer is formed over the second insulator layer exposing portions of the second insulator layer over: the planar ***copper interconnect*** bottom half of the stacked spiral inductor; a portion of the metal top plate and a portion of the planar ***copper interconnect*** contact portion of the MIM capacitor; and the two exposed planar ***copper***

interconnect routing points of the precision resistor. The second insulator layer is etched using the second patterned masking layer as a mask to form: an inductor trench exposing the planar ***copper interconnect*** routing points of the precision resistor; a MIM capacitor trench exposing the portion of the metal top plate and the portion of the planar ***interconnect*** contact point of the MIM capacitor; and routing point trenches exposing the two exposed planar ***copper interconnect*** routing points of the precision resistor. The inductor trench, the MIM capacitor trench and the routing point trenches are filled with planarized metal to complete the formation of: the spiral inductor within the spiral inductor area; the MIM capacitor within the MIM capacitor area; and the precision resistor within the precision resistor area.

USE - For integrating an integrated circuit component in ***copper interconnects***.

ADVANTAGE - The invention provides a cost effective method of integrating ***copper*** inductor, the MIM capacitor and the precision resistor in a ***copper*** integrated circuit fabrication process. It integrates the ***copper*** inductor, the MIM capacitor and the precision resistor in the ***copper*** IC fabrication process using conventional equipment and materials. It integrates the ***copper*** inductor, the MIM capacitor and the precision resistor in the ***copper*** IC fabrication process with minimal extra masking or processing. It produces high performance components (high inductor Q (quality)-factor, high capacitance capacitors, and low temperature coefficient (Tcr) resistors). It fabricates high performance IC passive components (the inductor, the MIM capacitor, and the precision resistor) compatible with ***copper interconnects*** and using conventional equipment and materials using a minimum of two masking steps. It requires minimal modifications to conventional ***copper*** damascene ***interconnect*** processes and uses as few as two additional masking layers to create the inductor, the resistor and the capacitor. It occurs after the standard digital wafer processing is completed and will not alter the digital behavior and design rule. The components are built in the top-most ***interconnect*** layer, or above, thus any coupling capacitance with the semiconductor substrate is minimized which becomes especially important at radio frequencies. A minimum of just one thin film deposition (for the resistor and for the capacitor top electrode) is required, thus resulting in a cost savings and a small topographic step (desirable for subsequent lithographic patterning without additional chemical mechanical polishing planarization.

DESCRIPTION OF DRAWING(S) - The figure is a plan view of an initial structure.

Spiral inductor area 12
MIM capacitor area 14
Precision resistor area 16
Exposed planar ***copper interconnect*** bottom half 22
Exposed planar ***copper interconnect*** routing points 24
Exposed planar ***copper interconnect*** bottom plate 26
Exposed planar ***copper interconnect*** contact point 28

Dwg.2/21

Technology

US 2002197844 A1UPTX: 20030529 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The metal layer over the first dielectric insulator layer is formed by a method from evaporation, chemical vapor deposition or ***physical vapor deposition***. A dielectric capping layer is formed over the metal layer over the first dielectric insulator layer. The patterned first masking layer formed over the metal layer also covers a portion of the area between the precision resistor are planar ***copper interconnect*** routing points. The etching of the metal layer over the first dielectric insulator layer uses a wet chemical etch process or a plasma etch process. An additional dielectric layer is formed over the metal layer over the first dielectric insulator layer. The diffusion barrier layer and

the metal layer over the first dielectric insulator layer are both etched using the patterned first masking layer. The second insulator is formed by a process from plasma etch chemical vapor deposition (PECVD) or a spin-on technique. A diffusion barrier metal layer ***lining*** is formed within the inductor trench, the MIM capacitor trench and the routing point trenches before filling the inductor trench, the MIM capacitor trench and the routing point trenches with the planarized metal. Preferred Component: The first dielectric insulator layer serves as both a metal diffusion barrier and the MIM capacitor dielectric. The wafer includes the MIM capacitor area. It does not include the precision resistor area. Preferred Property: The first dielectric insulator layer has a thickness of 200-1000 (preferably 600-700)Angstrom. The metal layer over the first dielectric insulator layer has a thickness of 200-700Angstrom. The dielectric capping layer has a thickness of 200-1000Angstrom. The second insulator has a thickness of is 0.5-5 mum. TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The first dielectric insulator layer comprises a material from silicon nitride (SiN, preferably), tantalum pentaoxide (Ta2O5), silicon oxynitride (SiON), hafnium oxide (HfO2), zirconium oxide (ZrO2), ***aluminum*** oxide (Al2O3), yttrium oxide (Y2O3), magnesium oxide and/or titanium dioxide (TiO2), high dielectric materials, or ferroelectric materials. The metal layer over the first dielectric insulator layer comprises a material from ***tantalum nitride*** (preferably), tantalum (preferably), titanium nitride, titanium tungstate (TiW), nickel-chromium (NiCr), molybdenum nitride, ***tungsten*** nitride, or ***tungsten*** silicon nitride. It preferably comprises a material from ***aluminum*** (***Al***) or an ***Al*** alloy having a thickness of 500-1500Angstrom. The dielectric capping layer comprises a material from SiN, silicon dioxide, or SiON. The second insulator comprises a material from silicon oxide, silicon dielectric material or organic low-dielectric constant (k) organic material.

☐ **L17 ANSWER 8 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-536472 [57] WPIX Full Text

Title

Barrier layer for interconnect structure, comprises layer of tantalum nitride in hexagonal phase between first material and second material isolated from each other.

Author/Inventor

CABRAL, C; DEHAVEN, P W; EDELSTEIN, D C; KLAUS, D P; POLLARD, J M; STANIS, C L; UZOH, C E

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002046874	A1	20020425	(200257)*		14	H01B017-00

Priority Application Information

US 1999-370003	**19990806**

International Patent Classification

ICM H01B017-00

Abstract

US2002046874 A UPAB: 20020906

NOVELTY - A barrier layer comprises a layer of ***tantalum nitride*** in hexagonal phase between a first material and a second material isolated from each other.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) ***Interconnection*** structure (10) which has a first insulation layer (12)

having an upper surface (14) and a lower surface (13) and having grooves (15) formed in upper surface. Some of grooves has regions extending to lower surface to expose conducting surfaces in a second ***interconnect*** structure below first insulation layer. A ***liner*** (23) including a layer of ***tantalum nitride*** hexagonal phase is formed on the sidewalls (27) and bottom (17) of grooves and on exposed conducting surfaces. A metal (24) is deposited on grooves to fill the grooves; and

(2) Gate stack over a channel of metal-oxide-semiconductor transistor which comprises a silica layer, a polycrystalline silicon layer, hexagonal ***tantalum nitride*** layer and a metal layer whose atoms are isolated from the polycrystalline silicon layer.

USE - For very large scale integration and ultra-large scale integration metal ***interconnects*** , ***studs*** for complementary metal-oxide semiconductor (CMOS) gate stacks on semiconductor chips, and for electrical ***interconnections*** in packaging and display devices.

ADVANTAGE - The barrier layer has good diffusion barrier performance, good adhesion to back end of the line (BEOL) insulators, good adhesion to ***interconnect*** metal and various dielectrics, such as polymers, silicon dioxide, borophosphosilicate glass and diamond-like carbon, low resistivity and stress, and good conformality in trenches and ***vias*** .

The barrier layer shields metal from gases such as corrosive ***tungsten*** hexafluoride used as a precursor gas for deposition of ***tungsten*** , and provides good contact resistance to preceding levels of metal, such as ***aluminum*** in BEOL wiring.

The barrier layer also provides better conformality than titanium-based compounds even without collimation ***sputtering*** or chemical vapor deposition.

The barrier layer also provides good conformality when deposited in trenches and ***vias*** BEOL structures. The barrier layer will not form a corrosion couple with ***copper*** , ***aluminum*** or ***tungsten*** during or after chemical mechanical polishing.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of the ***interconnect*** structure.

Interconnect structure 10
Insulation layer 12
Lower surface 13
Upper surface 14
Grooves 15
Semiconductor chip 16
Bottom 17
Liner 23 Metal 24
Sidewalls 27 Dwg.1/10

Technology

US 2002046874 A1UPTX: 20020906 TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The first material is ***copper*** , alloys of ***copper*** , ***aluminum*** , or alloys of ***aluminum*** , ***tungsten*** and lead-tin. The second material is silica, spin-on-glass, silicon nitride, polyamide, diamond-like carbon, fluorinated diamond-like carbon, ***tungsten*** silicide (WSi2), cobalt silicide (CoSi2), titanium silicide (TiSi2) or platinum silicide (PtSi). The metal is ***copper*** , ***aluminum*** , ***tungsten*** or their alloys, and the first insulation layer includes a material chosen from silica, spin-on-glass, silicon nitride, polyamide, diamond-like carbon or fluorinated diamond-like carbon. Preferred Properties: The ***tantalum nitride*** layer is highly oriented and has resistivity of 150-300 micro-ohm-cm or non-highly oriented and has a resistivity of more than 300 micro-ohm-cm. A tantalum layer is formed adjacent to or on the ***tantalum nitride*** layer, and is in alpha-phase and has resistivity of 15-60 micro-ohm-cm. and is in alpha-phase. Preferred Composition: The ***interconnector*** is formed on a semiconductor chip or a display device. A silicide layer is formed between the

polycrystalline silicon layer and the ***tantalum nitride*** layer, and atoms of metal layer are isolated from the silicide layer. The silicide layer comprises WSi2, CoSi2, TiSi2, PtSi or tantalum silicide (TaSi2).

☐ **L17 ANSWER 9 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-239118 [29] WPIX Full Text

Title

Formation of dual-damascene type conducting interconnect for microelectronics fabrication, involves forming non-metallic barrier over trench and via , before forming metallic barrier and copper layer on exposed conducting layer.

Author/Inventor

CHOOI, S; GUPTA, S; HONG, S; ZHOU, M

Patent Assignee/Corporate Source

(CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002001952	A1	20020103	(200229)*		19	H01L021-4763
US 6489233	B2	20021203	(200301)			H01L021-4763

Priority Application Information

US 2000-512379	**20000225**
US 2001-925821	20010810

International Patent Classification

ICM H01L021-4763

Abstract

US2002001952 A UPAB: 20030101

NOVELTY - A trench (22) and ***via*** (25) are patterned and etched through capping layer (20), dielectric layer (18), etch-stop layer (16), dielectric layer (14), extending to passivating layer (12).

A non-metallic barrier layer is formed over side walls of trench and ***via***. The conducting layer (10) is exposed by etching layer (12). A metallic barrier layer is formed on trench and ***via*** and ***copper*** is deposited over it.

DETAILED DESCRIPTION - A trench and ***via*** are patterned and etched through capping layer, dielectric layer (18), etch-stop layer, dielectric layer (14), extending to passivating layer. A non-metallic layer is formed over all surfaces of trench and ***via*** formation such that non-metallic layer conformally covers the layers. The portions of non-metallic layer is etched to form a barrier spacer over the side walls of trench and ***via*** formation and the exposed portion of passivation layer is etched to expose the conducting layer. A metallic barrier layer is formed over trench and ***via*** formation and ***copper*** is deposited over trench and ***via*** formation.

USE - For formation of dual-damascene type conducting ***interconnects*** such as ***copper*** damascene type ***interconnects*** , in microelectronics fabrication.

ADVANTAGE - Diffusion of fluorine from fluorinated dielectric materials into metallic barrier layer is prevented, thereby protecting ***interconnect liner*** from adverse effects of fluorine. Similarly diffusion of conducting materials such as ***copper*** , deposited in trenches and ***vias*** into surrounding dielectric materials and ***sputtering*** onto side walls of trenches and ***vias*** during etching, are avoided. ***Copper interconnects*** of reduced dimensions required in devices of sub-micron (0.15 mu) generation, is offered. A ***lining*** layer with low-k dielectric properties is formed which reduces problems associated with parasitic capacitance between conducting ***interconnects*** and other neighboring structures. The ***lining*** layer has improved adhesion properties between conductors and porous

dielectrics. A chemically inert spacer layer which protects surrounding materials from the effect of etches and post etched solvent stripping process, is formed.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of etched out trench and ***via*** of dual-damascene type ***interconnect***.

Conducting layer 10
Passivating layer 12
Dielectric layers 14,18
Etch-stop layer 16
Capping layer 20
Trench 22
Via 25 Dwg.4/20

Technology

US 2002001952 A1UPTX: 20020508 TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Structure: The conducting layer is ***copper*** layer of thickness 2000-15000 Angstrom and comprises ***aluminum*** -***copper*** alloy, ***tungsten*** , titanium or titanium oxide. The passivating layer, etch-stop layer and capping layer comprises silicon nitride and has thickness of 50-5000 Angstrom. The etch-stop layer comprises silicon oxy nitride. The dielectric layers (14,18) is a layer of fluorinated dielectric material of low dielectric constant (low-k) selected from FSG, Teflon, Parylene-F, amorphous fluorocarbon and fluorinated polyimide. The thickness of dielectric layer (14,18) is 1000-10000 Angstrom. The dielectric layer (18) alternately comprises undoped silica, carbon doped silicon oxide, organic polymer or inorganic polymer and its thickness is 1000-10000 Angstrom. The non-metallic layer comprises silicon carbide, boron nitride, carbon nitride, boron-carbon nitride, boron carbide and is formed by chemical vapor deposition or ***physical vapor deposition*** to a thickness of 500-5000 Angstrom. The plasma assisted etch for forming trench and ***via*** , comprises one or more gases selected from fluorocarbon(s), fluorine substituted hydrocarbon(s), fluoro sulfur, chlorine, hydrogen bromide, oxygen, nitrogen, argon, hydrogen and carbon monoxide. The non-metallic layer is etched using one or more gases selected from chlorine, boron trichloride, oxygen, hydrogen, nitrogen, forming gas (mixture of hydrogen and nitrogen), fluorocarbon(s), fluorine-substituted hydrocarbon(s) and argon. The plasma assisted etch used for etching passivation layer comprises hydrocarbon(s), fluorine substituted hydrocarbon(s), hydrocarbons, oxygen, nitrogen and argon. The metallic barrier layer contains tantalum, ***tantalum nitride*** , metal-silicon-nitride, titanium nitride and ***tungsten*** nitride and has thickness of 50-2000 Angstrom. Preferred Method: The trench and ***via*** formation is patterned and etched using the trench having width of 0.25-2.0 microns and then ***via*** having width of 0.15-0.4 microns, or using ***via*** and then trench or using self-alignment (buried ***via***) method. The non-metallic layer is a non-conductive layer comprising carbon based amorphous materials of varying composition, micro-structure and physical properties formed by plasma enhanced chemical vapor deposition or ***physical vapor deposition*** to a thickness of 100-3000 Angstrom. The non-conductive carbon-based amorphous material comprises carbon and optionally one or more non-metals. The non-conductive carbon-based layer preferably comprises fluorocarbon polymer, silicon carbide, carbon nitride and boron carbide. The dielectric layers and exposed surfaces of trench and ***via*** , are subjected to plasma treatment using gas mixture comprising one or more of nitrogen, ammonia and hydrazine, before forming the subsequent layers.

☐ **L17 ANSWER 10 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-239117 [29] WPIX Full Text

Title

Formation of dual-damascene type conducting interconnect for microelectronics

fabrication, involves forming non-metallic barrier over trench and via , before forming metallic barrier and copper layer on exposed conducting layer.

Author/Inventor

CHOOI, S; GUPTA, S; HONG, S; ZHOU, M

Patent Assignee/Corporate Source

(CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002001951	A1	20020103	(200229)*		19	H01L021-4763
US 6429122	B2	20020806	(200259)			H01L021-4763

Priority Application Information

US 2000-512379	**20000225**
US 2001-925820	20010810

International Patent Classification

ICM H01L021-4763

Abstract

US2002001951 A UPAB: 20020916

NOVELTY - A trench (22) and ***via*** (25) are patterned and etched through capping layer (20), dielectric layer (18), etch-stop layer (16), dielectric layer (14), till passivating layer (12). A non-metallic barrier layer is formed over side walls of trench and ***via***. The conducting layer (10) is exposed by etching layer (12). A metallic barrier layer is formed on trench and ***via*** , and ***copper*** is deposited over it.

DETAILED DESCRIPTION - A layered structure comprises conducting layer, passivating layer, dielectric layer (14), etch-stop layer, dielectric layer (18) and capping layer. A trench and ***via*** is patterned and etched on the layered structure extending till passivating layer. A non-metallic layer is formed over all surfaces of trench and ***via*** such that non-metallic layer con formally covers the layers. A portion of non-metallic layer is etched to form a barrier spacer over the side walls of trench and ***via*** , and the exposed portion of passivating layer is etched to expose the conducting layer. A metallic barrier layer is formed over all surfaces of trench and ***via*** , and ***copper*** is deposited over it.

USE - For formation of dual-damascene type conducting ***interconnects*** such as ***copper*** damascene type ***interconnects*** , in microelectronics fabrication.

ADVANTAGE - Diffusion of fluorine from fluorinated dielectric materials into metallic barrier layer is prevented, thereby protecting ***interconnect liner*** from adverse effects of fluorine. Similarly diffusion of conducting materials such as ***copper*** , deposited in trenches and ***vias*** into surrounding dielectric materials and ***sputtering*** onto side walls of trenches and ***vias*** during etching, are avoided. ***Copper interconnects*** of reduced dimensions required in devices of sub-micron (0.15 mu) generation, is offered. A ***lining*** layer with low-k dielectric properties is formed which reduces problems associated with parasitic capacitance between conducting ***interconnects*** and other neighboring structures. The ***lining*** layer has improved adhesion properties between conductors and porous dielectrics. A chemically inert spacer layer which protects surrounding materials from the effect of etches and post etched solvent stripping process, is formed.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of etched out trench and ***via*** of dual-damascene type ***interconnect***.

Conducting layer 10
Passivating layer 12
Dielectric layers 14,18
Etch-stop layer 16
Capping layer 20

Trench 22
Via 25 Dwg.4/20

Technology

US 2002001951 A1UPTX: 20020508 TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Composition: The conducting layer is ***copper*** layer of thickness 2000-15000 Angstrom and comprises ***aluminum*** -***copper*** , ***tungsten*** , titanium or titanium oxide. The passivating layer, etch-stop layer and capping layer comprise silicon nitride and each has thickness of 50-5000 Angstrom. Alternately, the etch-stop layer of thickness 500-5000 Angstrom comprises silicon oxy nitride. The dielectric layers (14,18) comprise fluorinated dielectric material of low dielectric constant (low-Mk) selected from FSG, Teflon, Parylene-F, amorphous fluorocarbon and fluorinated polyimide. The thickness of dielectric layers (14,18) is 1000-10000 Angstrom. The dielectric layer (18) alternately comprises undoped silica, carbon doped silicon oxide, organic polymer or inorganic polymer. The non-metallic layer comprises silicon carbide, boron nitride, carbon nitride, boron-carbon nitride, boron carbide and is formed by chemical vapor deposition or ***physical vapor deposition*** to a thickness of 500-5000 Angstrom. The plasma assisted etch for forming trench and ***via*** , comprises one or more gases selected from fluorocarbon(s), fluorine substituted hydrocarbon(s), fluoro sulfur, chlorine, hydrogen bromide, oxygen, nitrogen, argon, hydrogen and carbon monoxide. The non-metallic layer is etched using one or more gases selected from chlorine, boron trichloride, oxygen, hydrogen, nitrogen, forming gas (mixture of hydrogen and nitrogen), fluorocarbon(s), fluorine-substituted hydrocarbon(s) and argon. The plasma assisted etch used for etching passivating layer comprises hydrocarbon(s), fluorine substituted hydrocarbon(s), hydrocarbons, oxygen, nitrogen and argon. The metallic barrier layer contains tantalum, ***tantalum nitride*** , metal-silicon-nitride, titanium nitride and ***tungsten*** nitride and has thickness of 50-2000 Angstrom. Preferred Method: The trench and ***via*** is patterned and etched using the trench having width of 0.25-2.0 microns or 0.3-3.0 microns and then ***via*** having width of 0.1-0.4 microns, preferably 0.15-0.4 microns, or using ***via*** and then trench or using self-alignment (buried ***via***) method. A non-conductive layer may be formed instead of non-metallic layer over all surfaces of trench and ***via*** formation. The non-conductive layer comprises carbon based amorphous materials of varying composition, micro-structure and physical properties formed by plasma enhanced chemical vapor deposition or ***physical vapor deposition*** to a thickness of 100-3000 Angstrom. The non-conductive carbon-based amorphous material may comprise carbon and optionally one or more non-metals, or one among fluorocarbon polymer, silicon carbide, carbon nitride and boron carbide. The dielectric layers are formed using gas mixture comprising nitrogen, ammonia and hydrazine.

☐ **L17 ANSWER 11 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-127951 [12] WPIX Full Text

Title

Fabrication of integrated circuit to form alloyed copper interconnect lines and vias involves annealing using low temperature annealing step at specified temperature to enhance copper alloy formation of metal layer.

Author/Inventor

CHEN, S H; TSAI, M

Patent Assignee/Corporate Source

(TASE-N) TAIWAN SEMICONDUCTOR MFG CO

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6479389	B1	20021112	(200312)*		6	H01L021-302

Priority Application Information

US 1999-412632	**19991004**

International Patent Classification

ICM H01L021-302

Abstract

US 6479389 B UPAB: 20030603

NOVELTY - An integrated circuit (IC) on a substrate is fabricated to form alloyed ***copper interconnect*** lines and ***vias*** by annealing using a low temperature annealing step at 250-450 deg. C to enhance ***copper*** alloy formation (28) of metal layer.

DETAILED DESCRIPTION - Fabrication of IC to form alloyed ***copper*** (***Cu***) ***interconnect*** lines and ***vias*** involves:

(i) providing a substrate (20) or module with IC;

(ii) providing an ***interconnect*** wiring layer, or device contact regions to P-N junctions on the substrate;

(iii) providing a first layer of insulator (22) over the ***interconnect*** wiring layer, or device contact regions to P-N junctions;

(iv) providing patterned and etched ***via*** holes and trenches in the first layer of insulator;

(v) depositing a ***via*** hole and trench barrier ***liner*** material from ***tantalum nitride*** (***TaN***), titanium nitride (TiN) or ***tungsten*** nitride (WN) which is a diffusion barrier;

(vi) depositing by chemical vapor deposition or electrochemical deposition of a thick layer of pure ***Cu*** (26) over the barrier ***liner*** material planarizing the surface;

(vii) depositing an alloyed planar ***Cu*** layer from ***aluminum*** (***Al***), titanium (Ti), zinc (Zn) or ***Cu*** alloying metals by ***physical vapor deposition sputtering*** from an alloyed target;

(viii) annealing by a low temperature annealing step of 250-450 deg. C to enhance ***Cu*** alloy formation of all metal layer; and

(ix) polishing the excess conducting metal back by chemical mechanical polishing and repeating the above process steps to make multilevel conducting layers which are corrosion/oxidation and electromigration resistant.

USE - For fabricating IC on circuit to form alloyed ***Cu interconnect*** lines and ***vias***.

ADVANTAGE - The invention makes efficient use of processing steps resulting in less processing time, lower costs and higher device reliability. The unique ***copper*** metal alloyed conducting ***interconnect*** lines ***via*** structures produced have good adhesion properties with insulting films and resist both oxidation/corrosion and electromigration.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional representation of the annealing steps of ***Cu*** layers to form ***Cu*** alloys. Substrate 20
Insulator 22
Cu 26 Alloy layer 27
Copper alloy formation 28 Dwg.2c/2

Technology

US 6479389 B1 UPTX: 20030218 TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Component: The substrate is a semiconductor single crystal silicon. Preferred Material: The ***via*** hole and trench barrier ***liner*** material comprises a diffusion barrier ***liner*** which also aids adhesion, ***liner*** type material comprises ***TaN*** , TiN or WN with nitride formed by reactive ***sputtering***.

TECHNOLOGY FOCUS - CERAMICS AND GLASS - Preferred Component: The substrate is a ceramic module. TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The chemical vapor deposition or electro-chemical deposition of a thick layer of pure ***Cu*** planarizes the trench/***via*** surface and is a thickness of 3000-15000Angstrom. The alloyed planar ***copper*** layer, with a thickness 500-2500Angstrom is comprised of ***Cu*** alloying metals from ***Al*** , Ti or Zn, ***sputter*** deposited by ***physical vapor deposition*** forming alloy dopant compositions of 0.5-5.0 atm.% dopant in ***Cu*** , with 95-99.9 atm.% ***Cu***. Annealing by low temperature annealing of pure ***Cu*** and alloy layer (27) to enhance ***Cu*** metal alloy formation is performed in a low temperature of 250-450degreesC in an inert atmosphere or in a vacuum. The conducting structures are fabricating by repeating the integrated process to make multilevel conducting layer over the exposed ***Cu*** and ***Cu*** alloys during formation of the ***via*** holes and trench to prevent chemical attack. Each level of conducting structure is planarized by removing excess conducting material, including planarization by chemical mechanical polish or etching.

☐ **L17 ANSWER 13 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-862728 [80] WPIX Full Text

Title

Enclosing via in semiconductor device, by forming first the via and then trench in dielectric layer, both of them filled with respective metal liner , and covering the metal liners with metal layer.

Author/Inventor

EDWARDS, R D; FILIPPI, R G; IGGULDEN, R C; KIEWRA, E W; WANG, P

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6383920	B1	20020507	(200380)*		25	H01L021-4763

Priority Application Information

US 2001-757894	**20010110**

International Patent Classification

ICM H01L021-4763

Abstract

US 6383920 B UPAB: 20031211

NOVELTY - A ***via*** (216) is enclosed in a semiconductor device by forming first the ***via*** in a dielectric layer to expose portion of a first metal layer; depositing a first metal ***liner*** in the ***via*** ; forming trench (222) in the dielectric layer adjacent to the metal ***liner*** ; depositing a second metal ***liner*** in the trench; and depositing a second metal layer on the metal ***liners*** , thus filling the ***via*** and the trench.

DETAILED DESCRIPTION - Enclosure of ***via*** in a semiconductor device involves forming dielectric layer (214) on a first metal layer (206). A ***via*** is formed in the dielectric layer at a depth of at least equal to the thickness of the dielectric layer, thus defining a sidewall of the dielectric layer and exposing a portion of the first metal layer. A first metal ***liner*** (218) is deposited in the ***via*** . The metal ***liner*** includes a bottom portion deposited on the exposed portion of the first metal layer and a sidewall portion of the first metal layer. At least one trench is formed in the dielectric layer adjacent to the first metal ***liner***. It has a depth of less than the thickness of the dielectric layer, thus defining trench bottom and sidewall and exposing an upper portion of the sidewall portion of the first metal ***liner***. A second metal ***liner*** (224) is

deposited in the trench, preferably at the bottom and sidewall of the trench. A second metal layer (226) is deposited on the first and second metal ***liners*** , thus filling the ***via*** and the trench.

USE - For enclosing a ***via*** in a semiconductor device.

ADVANTAGE - The method reduces void formation due to electromigration, thus improving reliability in dual damascene ***interconnects***.

DESCRIPTION OF DRAWING(S) - The figures are cross-sectional views of wafer stack.

Metal layer 206, 226

Dielectric layer 214

Via 216

Metal ***liner*** 218, 224 Trench 222

2E, 2G/4

Technology

US 6383920 B1 UPTX: 20031211 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The dielectric layer is formed by chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), ***physical vapor deposition*** (***PVD***), high density plasma chemical vapor deposition (HDPCVD), or spin-on glass deposition. The ***via*** and trench are formed by photolithography process. The metal ***liners*** are deposited by ***sputter*** deposition, CVD, ***PVD*** , or ionized ***physical vapor deposition***. The second metal layer is deposited by CVD, PECVD, ***PVD*** , ***sputter*** deposition, electroplating, or electroless plating. Preferred Component: The dielectric layer comprises first oxide layer, a hardmask layer, or a second oxide layer. Preferred Dimension: The dielectric layer is a 0.4-2 micrometers thick. The first and second oxide layer are each 0.2-1 micrometers thick. The hardmask layer is 50-500 Angstrom thick. The metal ***liner*** are each 10-1000 Angstrom, preferably 25-100 Angstrom thick.

TECHNOLOGY FOCUS - METALLURGY - Preferred Material: The first metal layer comprises ***aluminum*** , ***copper*** , ***tungsten*** , gold, silver, or their alloys. The metal ***liners*** comprise refractory metal or refractory metal nitride, preferably titanium, titanium ***nitride*** , ***tantalum*** , ***tantalum nitride*** , ***tungsten*** , ***tungsten*** nitride, titanium silicon nitride, ***tungsten*** nitride, or their alloys. The second metal layer comprises ***aluminum*** , ***copper*** , ***tungsten*** , gold, silver, or their alloys.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The dielectric layer comprises silicon dioxide, fluorosilicate glass, silicon nitride, diamond-like carbon, or nano-pore containing material. The first and second oxide layer are each formed of silicon dioxide. The hardmask comprises silicon nitride or silicon oxynitride. TECHNOLOGY FOCUS - POLYMERS - Preferred Material: The dielectric layer may also comprise polyimide, parylene, polytetrafluoroethylene, polymer-based low-k dielectric material, or benzocyclobutene.

☐ **L17 ANSWER 14 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-572764 [61] WPIX Full Text

Title

Fabrication of wire bonds on pure copper damascene for e.g. complementary metal oxide semiconductor devices, involves forming aluminum -copper bond alloy on top of underlying copper pad metal.

Author/Inventor

CHOOI, S; HONG, S; ZHOU, M S

Patent Assignee/Corporate Source

(CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6376353	B1	20020423	(200261)*		18	H01L021-44

Priority Application Information

US 2000-609167	**20000703**

International Patent Classification

ICM H01L021-44
ICS H01L021-302; H01L021-4763

Abstract

US 6376353 B UPAB: 20020924
NOVELTY - Wire bonds are fabricated on pure ***copper*** damascene by forming ***aluminum*** -***copper*** bond alloy on top of underlying ***copper*** pad metal.

DETAILED DESCRIPTION - Fabrication of wire bonds involves:

(1) depositing a passivating layer over a first level of conducting wiring (4) defined and over a substrate (1) wafer or module;

(2) depositing two insulating layers forming intermetal dielectric (IMD) layers, patterning and etching the intermetal dielectric layers (14, 16) and passivating layer to form a dual damascene trench (20)/***via*** (19) opening exposing regions of the conducting wiring;

(3) depositing and patterning a cap layer over the second IMD layer;

(4) depositing a first blanket conductive metal barrier layer or first barrier layer over the patterned cap layer and into the trench/ ***via*** openings and over the exposed regions of the conducting wiring;

(5) depositing a blanket ***copper*** layer over the first barrier layer and filling the trench/***via*** opening;

(6) polishing back by chemical mechanical polishing (CMP) the excess ***copper*** and first barrier layer material (13) stopping on the cap layer to form a dual damascene inlaid ***copper*** in trench/ ***via*** opening;

(7) selectively wet etching the top layer of the inlaid ***copper*** to form a recessed ***copper*** and partially recessed trench/***via*** opening;

(8) etching ***copper*** oxide on the top layer of the recessed ***copper*** by hydrogen ammonia or ammonia plasma gas treatment;

(9) depositing a second blanket conductive metal barrier layer or second barrier layer (33) over the recessed ***copper*** and patterned cap layer;

(10) depositing a blanket layer of ***aluminum*** -***copper*** alloy (26, 34) over the second barrier layer and filling partially recessed trench/***via*** opening;

(11) annealing thermally with forming gas the alloy; and

(12) polishing back by CMP the alloy and second barrier layer material stopping on the cap layer (17, 27) to form a region of inlaid alloy.

USE - For fabricating wire bonds on pure ***copper*** damascene used for metal oxide field effect transistor and complementary metal oxide semiconductor devices and for both memory and logic device applications.

ADVANTAGE - The invention improves wire bond adhesion to the bond pad and prevents peeling during wire bond adhesion tests. It has very low failure rates and shows a high reliability, as tested by gold wire bond pull tests. It is free from stress-attack, corrosion, peeling, interface failure and adhesion failures. The top ***aluminum*** -***copper*** bond layer can be soldered without the need for further passivation.

DESCRIPTION OF DRAWING(S) - The figures show cross-sectional views of the invention.

Substrate 1
Wiring 4
First barrier layer material 13
Intermetal dielectric layers 14, 16 Cap layer 17, 27
Via 19 trench 20

Aluminum **-*copper*** alloy 26, 34
Second barrier layer 33
3d, 4d/5

Technology

US 6376353 B1 UPTX: 20020924 TECHNOLOGY FOCUS - ORGANIC CHEMISTRY - Preferred Method: The top ***copper*** layer is selectively etched by wet etching using dimethylsulfoxide (DMSO)/carbon tetrachloride (CCl4) solution, DMSO, or CCl4 at 20-150 degrees C for 5-100 Angstrom/minute for 1-60 minutes for a ***copper*** removal of 100-8000 Angstrom. It can be etched using hydrofluoric acid (HF), acetic acid (CH3COOH), ammonium fluoride (NH4F), tetramethylammonium hydroxide (TMAH), tetraethylammonium hydroxide (TEAH), tetrapropylammonium hydroxide (TPAH), benzotriazole, surfactant, or water (H2O). It can also be etch by using HF/CH3COOH, HF/NH4F/H2O, HF/NH4F/H2O/surfactant, or TMAH/H2O. TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The substrate is a semiconductor or an integrated circuit module. The substrate comprises mono-crystalline silicon with semiconductor structure device structures from gate electrodes, source and drain regions, metal ***interconnects*** , damascene ***interconnects*** , contact holes, or ***vias*** , formed in and on the substrate. The bond pad is over a dual damascene ***interconnect*** trench/***via*** filled with ***copper*** and ***lined*** with a diffusion barrier layer. Preferred Method: An etch stop layer is formed on the first insulating layer of dielectric. The second barrier layer is deposited by ***physical vapor deposition*** or chemical vapor deposition. The blanket layer is deposited on the second barrier layer by ***physical vapor deposition*** or ***sputtering*** for a film thickness of 2000-20000 Angstrom, using direct current magnetron ***sputtering*** with argon gas at 0.1-10000 mTorr, 100-10000 Watts, 25-500 degrees C and argon gas flow of 0.1-100 sccm. The forming gas annealing the alloy layer comprises a gas ambient of a mixture of nitrogen and hydrogen gas or forming gas temperature of 200-500 degrees C at 20-60 minutes, and 400-760 Torr. The bond pad layer and second barrier layer are centrally patterned and formed by a reactive ion etching back using chloride/boron chloride, or the excess ***aluminum*** ***-copper*** and second barrier material are removed by chemical mechanical polishing and for both methods stopping on the silicon nitride cap layer. The bond pad is planarized by removing excess conducting material using chemical mechanical polishing, milling, ion milling, and/or etching leaving only the ***aluminum*** ***-copper*** on the ***copper*** dual damascene inlaid structures including trench/ ***via*** and ***interconnect*** portions, stopping on the cap layer. Preferred Property: The cap layer has a thickness of approximately 500-6000 Angstrom. The second barrier layer has a thickness of approximately 20-5000 Angstrom. The bond pad comprises a bond pad size, width, and length of approximately 1 by 1 micrometer to the power 2 to 1000 by 1000 micrometer to the power 2.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Component: The passivating cap layer is silicon nitride, silicon oxynitride, silicon carbide, or boron nitride. The second barrier layer is tantalum, ***tantalum nitride*** , titanium nitride, or ***tungsten*** nitride.

TECHNOLOGY FOCUS - METALLURGY - Preferred Composition: The bond pad layer comprises 99.99-90 wt.% ***aluminum*** metal and 0.01-10 wt.% ***copper*** metal.

☐ **L17 ANSWER 15 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2000-678683 [66] WPIX Full Text

Title

Fabrication of an integrated circuit involves doing special patterning process on the second etch stop layer by partially removing the etch stop barrier over the via and leaving the second etch stop barrier for trench.

Author/Inventor

SHUE, S; TSAI, M

Patent Assignee/Corporate Source

(TASE-N) TAIWAN SEMICONDUCTOR MFG CO

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6133144	A	**20001017**	(200066)*		11	H01L021-4763

International Patent Classification

ICM H01L021-4763

Abstract

US 6133144 A UPAB: 20001219

NOVELTY - An integrated circuit is fabricated on a substrate by performing a special patterning process on the second etch stop layer on top of the first intermetal dielectric layer (IMD) deposited over the first etch layer on top of the first level wiring layer and insulating layer. The stop layer material is removed over the ***via*** and patterned so that a stop layer material is left in trench areas.

DETAILED DESCRIPTION - Fabrication of the integrated circuit on the substrate (10) involves performing a special patterning process on the second etch stop layer on top of the first intermetal dielectric layer (IMD) (17) deposited over the first etch layer (16) on top of the first level wiring layer and insulating layer (14). The second etch stop layer material is removed over the ***via*** and patterned so that a stop layer material is left in trench or channel areas. A second IMD (30) is deposited over the patterned etch barrier which is patterned and etched to form special ***interconnect /via*** structures (44) and ***interconnect*** structures (46). The remnant etch stops are removed by a selective etch process. A channel and ***via*** barrier ***liner*** material is deposited in addition to the conducting material. The excess is polished back using chemical mechanical polishing. The process steps are repeated to construct multilevel conducting layers. The substrate where the integrated circuit is fabricated has a layer dielectric, interlevel dielectric (11), an ***interconnect*** line layer, or device contact region to P-N junctions.

USE - For fabricating integrated circuits, unique ***interconnect*** conducting lines, and ***via*** contact structures.

ADVANTAGE - The process produces well-defined, special low parasitic capacitance structures. It produces a reliable product with superior lines and ***via*** contact structures. It also reduces processing time and cost of ownership.

DESCRIPTION OF DRAWING(S) - The figure shows the formation of ***interconnect /via*** and ***interconnect*** wiring structures.

Substrate 10

Interlevel dielectric 11

Insulating layer 14

First etch layer 16

First intermetal dielectric layer (IMD) 17 Second IMD 30

Interconnect /via structures 44

Interconnect structures 46 Dwg.4/4

Technology

US 6133144 A UPTX: 20001219 TECHNOLOGY FOCUS - CERAMICS AND GLASS - Preferred Material: The substrate is semiconductor single crystal silicon or is a ceramic module with integrated circuits.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The layers of etch stop barriers are semiconductors, intermetallics, metals, or low dielectric films comprising refractory materials consisting of silicon nitride or silicon oxynitride, having very different etch properties than silicon oxide for

selective etching. The ***liner*** type materials comprise titanium, titanium nitride, ***tungsten*** or ***tantalum nitride***. The conducting material layers for conducting ***interconnect*** lines and the ***via*** contacts comprise ***aluminum*** , ***copper*** or ***aluminum copper*** silicate (AlCuSi). The first etch stop barrier materials comprise combined SixNy and/or silicon oxynitride. The second etch stop barrier materials comprise ***tantalum nitride*** or titanium nitride. Preferred Property: Silicon nitride and/or silicon oxynitride is plasma enhanced chemical vapor deposited to the first etch stop layer at a thickness of 100-1,000Angstrom. ***Tantalum nitride*** and/or titanium nitride is reactive ***sputter*** deposited to the second etch stop layer to a thickness of 30-500Angstrom. Silicon oxide is plasma enhanced chemical vapor deposited to the intermetal dielectric layers to a thickness of 1,000-20,000Angstrom. TECHNOLOGY FOCUS - ELECTRONICS - Preferred Structure: The combination ***interconnect /via*** structure and ***interconnect*** structures is unique, special, self aligned, with low parasitic capacitance formed using a self aligned dual damascene process with special patterning comprising two etch stop barrier layers, two intermetal dielectric layers, two patterning steps and three selective etch steps. Preferred Method: The highly selective patterned etches comprise critical process controls for all etch steps, with the use of fine tuning the etch selectivity and the use of endpoint signal detection methods. The highly selective etch steps are performed using both the large etch differences between the silicon oxide and silicon nitride and the specially patterned structures of the double level etch barrier stop layers. Each level of conducting structure is planarized by removing excess conducting material. Planarization is done by chemical mechanical polish or etching.

☐ **L17 ANSWER 16 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2002:658531 HCAPLUS Full Text

Title

Low-k interconnect structure comprised of a multilayer of spin-on porous dielectrics

Author/Inventor

Gates, Stephen Mcconnell; Hedrick, Jeffrey Curtis; Nitta, Satyanarayana V.; Purushothaman, Sampath; Tyberg, Christy Sensenich

Patent Assignee/Corporate Source

International Business Machines Corporation, USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002117760	A1	20020829	2001-795431	**20010228**
US 6603204	B2	20030805		
WO 2002071467	A1	20020912	2001-US45816	20011204
EP 1371091	A1	20031217	2001-990800	20011204
TW 544845	B	20030801	2002-91103304	20020225
US 2003075803	A1	20030424	2002-292205	20021112
US 6716742	B2	20040406		
US 2003183937	A1	20031002	2003-396274	20030325

Abstract

A low-k dielec. metal conductor ***interconnect*** structure having no micro-trenches present therein and a method of forming such a structure are provided. Specifically, the above structure is achieved by providing an ***interconnect*** structure which includes at least a multilayer of dielec. materials which are applied sequentially in a single spin apply tool and then cured in a single step and a plurality of patterned metal conductors within the multilayer of spun-on dielecs. The control over the conductor resistance is obtained using a buried etch stop layer having a 2nd atomic composition located between the line and ***via*** dielec. layers of porous low-k dielecs. having a 1st atomic composition The inventive ***interconnect*** structure also includes a hard mask which assists in forming the ***interconnect*** structure of the dual damascene-type. The 1st and 2nd composition are selected to obtain etch selectivity of 10:1 or higher, and are selected from specific groups of porous low-k organic or inorg. materials with specific atomic compns. and other discoverable quantities.

Controlled or Index Terms

Interconnections , electric
(multilayer; low-k ***interconnect*** structure comprised of a multilayer of spin-on porous dielecs.)

Etching
(***sputter*** , ion-beam, reactive; low-k ***interconnect*** structure comprised of a multilayer of spin-on porous dielecs.)

Aluminum alloy, base

Copper alloy, base

Silver alloy, base

Tungsten alloy, base

RL: PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(conductive layer; low-k ***interconnect*** structure comprised of a multilayer of spin-on porous dielecs.)

84540-57-8, Propylene glycol methyl ether acetate

RL: NUU (Other use, unclassified); USES (Uses)
(adhesion promoter; low-k ***interconnect*** structure comprised of

a multilayer of spin-on porous dielecs.)
7440-33-7 , Tungsten , processes
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(conductive layer, ***liner*** material, ***liner*** material; low-k ***interconnect*** structure comprised of a multilayer of spin-on porous dielecs.)
7429-90-5 , Aluminum , processes 7440-22-4, Silver, processes ***7440-50-8 , Copper*** , processes
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(conductive layer; low-k ***interconnect*** structure comprised of a multilayer of spin-on porous dielecs.)
7440-03-1, Niobium, processes 7440-25-7, Tantalum, processes
7440-32-6, Titanium, processes 7440-47-3, Chromium, processes
12033-62-4 , Tantalum nitride (TaN)
12058-38-7, ***Tungsten*** nitride (WN) 25583-20-4, Titanium nitride (TiN)
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(***liner*** material; low-k ***interconnect*** structure comprised of a multilayer of spin-on porous dielecs.)
78-10-4, Tetraethoxysilane
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(low-k ***interconnect*** structure comprised of a multilayer of spin-on porous dielecs.)
203945-07-7, Silk (dielectric) 334490-64-1, HOSP
RL: TEM (Technical or engineered material use); USES (Uses)
(low-k ***interconnect*** structure comprised of a multilayer of spin-on porous dielecs.)

Supplementary Terms

multilayer ***interconnection*** structure spin on porous dielec

International Patent Classification

ICM H01L021-4763
ICS H01L023-48; H01L029-40

☐ **L17 ANSWER 17 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2002:658527 HCAPLUS Full Text

Title

Hybrid low-k interconnect structure comprised of 2 spin-on dielectric materials

Author/Inventor

Gates, Stephen Mcconnell; Hedrick, Jeffrey Curtis; Nitta, Satyanarayana V.; Purushothaman, Sampath; Tyberg, Christy Sensenich

Patent Assignee/Corporate Source

International Business Machines Corporation, USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002117754	A1	20020829	2001-795429	**20010228**
US 6677680	B2	20040113		

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2002071468	A1	20020912	2001-US47794	20011210
EP 1371090	A1	20031217	2001-990106	20011210
JP 2004523910	T2	20040805	2002-570287	20011210
TW 533544	B	20030521	2002-91103227	20020222

Abstract

The present invention relates to ***interconnect*** structures for high-speed microprocessors, application specific integrated circuits (ASICs) and other high-speed integrated circuits (ICs). The present invention provides low dielec. constant, i.e., low-k, ***interconnect*** structures having enhanced circuit speed, structure stability during thermal cycling, precise values of conductor resistance, reduced fabrication cost, and improved ease of processing due to chemical-mech. polishing (CMP) compatibility. Moreover, the inventive structures have a lower effective dielec. constant and improved control over metal line resistance as compared to conventional structures of the prior art. A metal wiring plus low-k dielec. ***interconnect*** structure of the dual damascene-type is provided in which the conductive metal lines and ***vias*** are built into a hybrid low-k dielec. which includes 2 spun-on dielecs. that have different atomic compns. and ≥1 of the 2 spun-on dielecs. is porous. The 2 spun-on dielecs. used in forming the inventive hybrid low-k dielec. each have a dielec. constant of .apprx.2.6 or less, preferably each dielec. of the hybrid structure has a k of from .apprx.1.2 to .apprx.2.2. By using the inventive hybrid low-k dielec. excellent control over metal line resistance (trench depth) is obtained, without no added cost. This is achieved without the use of a buried etch stop layer, which if present, would be formed between the 2 spun-on dielecs. Also, the spun-on dielecs. of the hybrid low-k dielec. have distinctly different atomic compns. enabling control over the conductor resistance using the bottom spun-on dielec. (i.e., ***via*** dielec.) as an inherent etch stop layer for the upper spun-on dielec. (i.e., line dielec.).

Controlled or Index Terms

Integrated circuits
Interconnections , electric
Sputtering
(hybrid low-k ***interconnect*** structure comprised of 2 spin-on dielec. materials)
Vapor deposition process
(plasma; hybrid low-k ***interconnect*** structure comprised of 2 spin-on dielec. materials)
Aluminum alloy, base
Copper alloy, base
Silver alloy, base
Tungsten alloy, base
RL: DEV (Device component use); USES (Uses)
(conductive layer; hybrid low-k ***interconnect*** structure comprised of 2 spin-on dielec. materials)
7440-33-7 , ***Tungsten*** , uses
RL: DEV (Device component use); USES (Uses)
(conductive layer, ***liner*** material; hybrid low-k ***interconnect*** structure comprised of 2 spin-on dielec. materials)
7429-90-5 , ***Aluminum*** , uses 7440-22-4, Silver, uses
7440-50-8 , ***Copper*** , uses
RL: DEV (Device component use); USES (Uses)
(conductive layer; hybrid low-k ***interconnect*** structure comprised of 2 spin-on dielec. materials)
7440-03-1, Niobium, uses 7440-25-7, Tantalum, uses 7440-32-6,

Titanium, uses 7440-47-3, Chromium, uses ***12033-62-4*** , ***Tantalum nitride*** (***TaN***) 12058-38-7, ***Tungsten*** nitride (WN) 25583-20-4, Titanium nitride (TiN)
RL: DEV (Device component use); USES (Uses)
(***liner*** material; hybrid low-k ***interconnect*** structure comprised of 2 spin-on dielec. materials)

Supplementary Terms
spin on dielec film hybrid ***interconnection*** structure

International Patent Classification
ICM H01L023-48
ICS H01L023-52; H01L029-40

☐ **L17 ANSWER 18 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number
2001:294942 HCAPLUS Full Text

Title
Combined chemical mechanical polishing and reactive ion etching process for semiconductor substrates

Author/Inventor
Ference, Thomas G.; Landers, William F.; MacDonald, Michael J.; Mlynko, Walter E.; Murray, Mark P.; Peterson, Kirk D.

Patent Assignee/Corporate Source
International Business Machines Corp., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6221775	B1	20010424	1998-159699	**19980924**
KR 2000023003	A	20000425	1999-38259	19990909

Abstract
A process is provided for planarizing the surface of a semiconductor substrate. The process begins by forming patterned raised and recessed regions on the surface of the semiconductor substrate. A layer of material then is formed over the patterned raised and recessed regions. The layer is subjected to a chemical mech. planarizing (CMP) process step until all of the raised regions are at least partially removed from the layer. Finally, the surface of the polished substrate is etched with a reactive ion etching (RIE) process.

Controlled or Index Terms
Polishing
(chemical-mech.; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
Vapor deposition process
(chemical; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
Contact holes
Integrated circuits
Semiconductor device fabrication
(combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
Vapor deposition process
(plasma; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
Electric contacts
(plugs; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
Etching

(***sputter*** , ion-beam, reactive; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
Aerogels
(substrate; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
Borophosphosilicate glasses
Phosphosilicate glasses
RL: TEM (Technical or engineered material use); USES (Uses)
(substrate; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
Interconnections (electric)
(***via*** ; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
1306-38-3, Ceria, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(abrasive; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
409-21-2, Silicon carbide, processes 7440-25-7, Tantalum, processes
7440-32-6, Titanium, processes ***12033-62-4*** , ***Tantalum nitride*** (***TaN***) 12033-89-5, Silicon nitride, processes
25583-20-4, Titanium nitride (TiN)
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(chemical-mech. polishing ***liner*** layer; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
7429-90-5 , ***Aluminum*** , uses ***7440-33-7*** , ***Tungsten*** , uses ***7440-50-8*** , ***Copper*** , uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(device conductive layer; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)
7631-86-9, Silica, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(substrate; combined chemical mech. polishing and reactive ion etching process for semiconductor substrates)

Supplementary Terms

semiconductor device fabrication chem mech polishing reactive ion etching

International Patent Classification

ICM H01L021-302

☐ **L17 ANSWER 19 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1999:468166 HCAPLUS Full Text

Title

Continuous highly conductive metal wiring structures and fabrication of same

Author/Inventor

Uzoh, Cyprian E.

Patent Assignee/Corporate Source

International Business Machines Corporation, USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5930669	A	**19990727**	1997-838222	19970403
JP 10284603	A2	19981023	1998-87234	19980331

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2999991	B2	20000117		

Abstract

The present invention relates to a method of fabricating wiring structures which contain a continuous, single crystalline conductive material extending through the structure. This is achieved by utilizing an open-bottomed ***via liner*** structure.

Controlled or Index Terms

Contact holes
Electric conductors
Electric contacts
Interconnections (electric)
Semiconductor device fabrication
(continuous highly conductive metal wiring structures and fabrication of same)
Metals, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(continuous highly conductive metal wiring structures and fabrication of same)
Sputtering
Sputtering
(etching, ion-beam, reactive; continuous highly conductive metal wiring structures and fabrication of same)
Sputtering
Sputtering
(etching, ion-beam; continuous highly conductive metal wiring structures and fabrication of same)
Etching
Etching
(***sputter*** , ion-beam, reactive; continuous highly conductive metal wiring structures and fabrication of same)
Etching
Etching
(***sputter*** , ion-beam; continuous highly conductive metal wiring structures and fabrication of same)
7440-50-8 , ***Copper*** , properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(continuous highly conductive metal wiring structures and fabrication of same)
7429-90-5 , ***Aluminum*** , uses 7440-25-7, Tantalum, uses
7440-32-6, Titanium, uses ***7440-33-7*** , ***Tungsten*** , uses
7440-47-3, Chromium, uses ***12033-62-4*** , ***Tantalum nitride*** (***TaN***) 37258-28-9 59124-10-6
RL: TEM (Technical or engineered material use); USES (Uses)
(***liner*** ; continuous highly conductive metal wiring structures and fabrication of same)

Supplementary Terms

conductor metal wiring structure fabrication; semiconductor device fabrication conductor metal wiring

International Patent Classification

ICM H01L021-00